Eidgenössische Technische Hochschule Zürich

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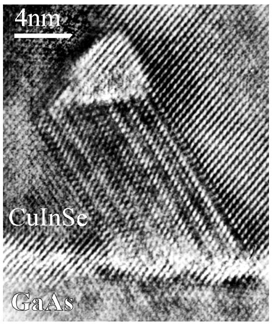
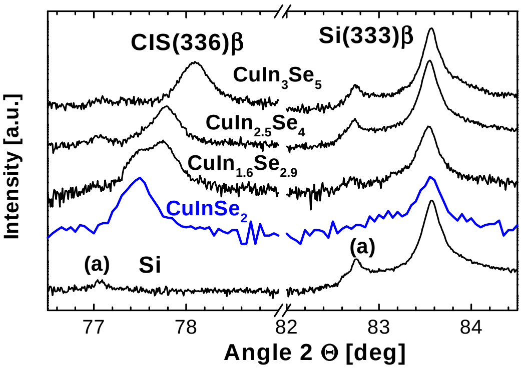
Annual Report Jahresbericht 1999

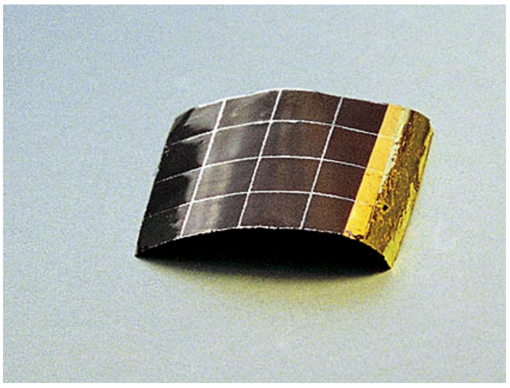
Gruppe Dünnschichtphysik

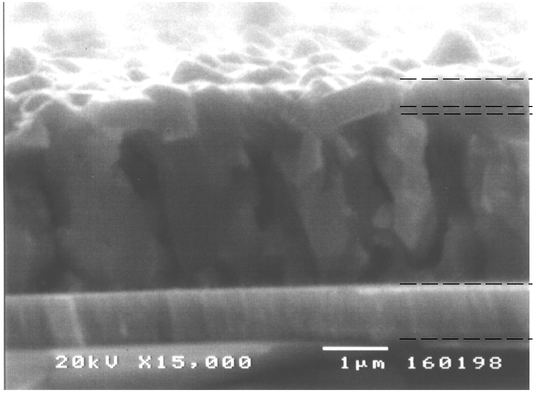
Thin Film Physics Group



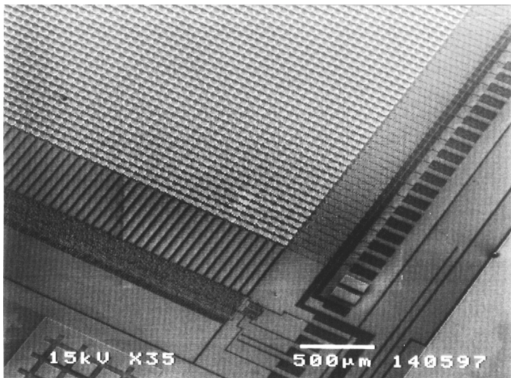


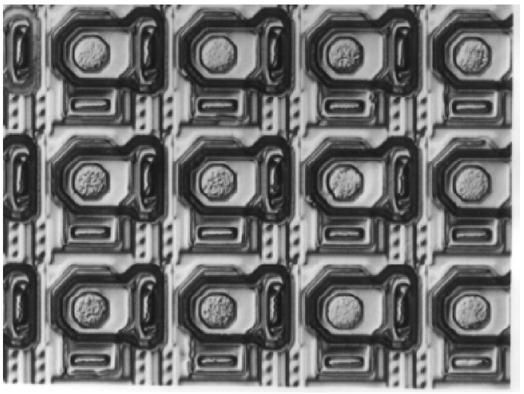
HRTEM of CIS/GaAs *XRD of CIS-phases*





CIGS solar cell on plastic substrate with 12.8% efficiency, cross section of a CIGS-structure





2-dimensional infrared sensor array and enlarged view of some individual pixels content:

GENERAL

The thin film physics group was integrated into the Institute of Quantum Electronics in Mai 1997, after the organisation AFIF (Arbeitsgemeinschaft für industrielle Forschung) to which the group belonged for many years was closed.
As before, the group is financed by projects ("Drittmittel") only, including all positions. The projects are financed by SNF, KTI, GRD, BBW (EU-Projects) and industry. Typical project durations are 2-3 years.

EQUIPMENT

4 MBE-chambers with solid state sources for CaF_2 ,$Pb_{1-x}Sn_xSe$, $CuIn_xGa_ySe_z$, and CdTe
6 PVD for sample sizes up to 20 x 20 cm^2, thermal and e-beam evaporation
3 sputtering chambers, DC and RF
complete photolithographic processing equipment
bonder
profilometer
light microscopy, SEM, XRD
electrooptic characterization for infrared sensors and solar cells

COLLABORATERS

Head: *PD Dr. Hans Zogg*

Group leader projects on solar cells: *Dr. Ayodhya N. Tiwari*

Postdocs:	*n.n**.***	
Ph.D students:	*Karim Alchalabi*	*(Doktorvater: Prof. Dr. G. Kostorz)*
	Franz Haug	*(Doktorvater: Prof.Dr. H. Melchior)*
	Dominik Rudmann	*(Doktorvater: Prof. G. Kostorz)*
	Allessandro Romeo	*(Doktorvater: Prof. Dr. H. Melchior)*
	Derk Bätzner	*(Doktorvater: Prof. Dr. L. Gaukler)*
Technicians:	*Michael Leopold*	*(60%)*
	n.n. (60%)	
	Gerhard Schreiber	*(10%)*
Secretary:	*Paulette Pfammatter*	*(10%)*

RESEARCH FIELDS

1. Science and technology of compound semiconductors:
Growth of molecular beam epitaxial (MBE) and polycrystalline layers of II-VI, IV-VI, I-III-VI_2, and III-V binary and multinary compounds. Applications for optoelectronic devices. Growth kinetics of heterostructures, superlattices and nano-structures (quantum dots). Phase formation and their identification.

Structural properties of thin films, surfaces and interfaces. Crystallographic and microstructural defects. Lattice vibrational properties of semiconductors. Measurement and modelling of strain relaxation in thin films. Kinetics of dislocation-glide and -reactions in IV-VI-on-Si epitaxial layers. Recrystallization in semiconductors.

Optical and electrical properties of thin films and heterostructures. *in-situ* and *ex-situ* doping in semiconductors, electronic defects and transport properties.

Growth, properties and applications of transparent conducting oxides (ZnO, ITO, TO).

Growth and properties of permeation barrier layers ("flexible glass" on plastics).

Thin film growth processes like molecular beam epitaxy, e-beam evaporation, d.c. and r.f. sputtering, chemical bath deposition, electro-deposition, etc.

2. Infrared detector arrays on Silicon substrates:
MBE growth of narrow gap IV-VI layers (lead chalcogenides) on Si-substrates. Fabrication of 1-d and 2-d IR sensor arrays; the Si-substrate may contain integrated read-out circuits. Development of microlithographic patterning techniques. Applications include thermal imaging and IR-spectrometry.

3. Compound semiconductor thin film solar cells:
Solar cells based on Cu(In,Ga)Se_2 and CdTe (these materials yield most stable and very high efficiency solar cells for economical production of solar electricity). Development of fabrication processes, novel materials and processes for improved performance and advanced tandem devices. Interface and transport properties of heterojunctions.
Studies of basic material properties and heterostructures for large area and industrial production. Stability and reliability of devices. Terrestrial and space applications of lightweight and flexible thin film solar cells.

4. Bragg reflectors:
MBE-growth of quarter-wavelengths stacks for Bragg mirrors with very high reflectivity *and* bandwidth by use of high/low index pairs like IV-VI or III-V semiconductors and group-IIa fluorides.

Some highlights:

- World record efficiency (12.8%) for a flexible Cu(In,Ga)Se_2 thin film solar cell
- Processes for polycrystalline Cu(In,Ga)Se_2 thin film solar cells on glass substrates with ~15% efficiency established
- CdTe solar cells of 12.5% efficiency with vacuum evaporation and new stable ohmic contatcs
- Epitaxial growth of chalcopyrite $CuInSe_2$ and defect-chalcopyrite $CuIn_3Se_5$ on Si for the first time. Identification of a $CuIn_{2.5}Se_4$ phase.
- Highly transparent ($T_{visible}$ >85%) and conducting (sheet resistance < 10 Ω/□) ZnO:Al layers grown by RF magnetron sputtering
- High resolution transmission electron microscopy and RBS for microstructural defects and compound formation at the interface of $CuIn_xSe_y$ with Si and GaAs
- Development of 1- and 2-dimensional infrared sensor arrays for thermal imaging in e.g. epitaxial PbTe on Si-substrates which contain active circuits
- Extreme dislocation motion and reduction ($<10^6$ cm^{-2}) in lattice mismatched epitaxial IV-VI semiconductor layers on Si(111)

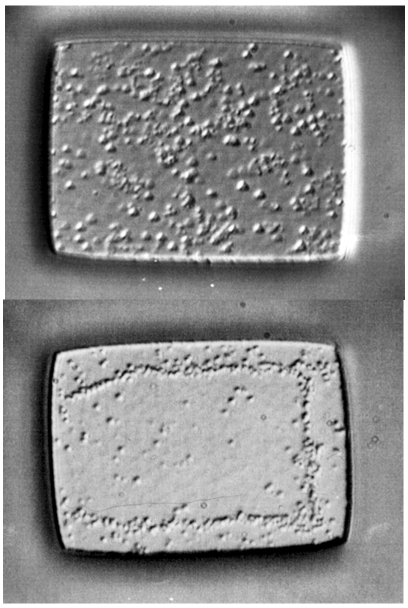
Epitaxial Narrow gap Lead Chalcogenide Layers on Si-Substrates for Infrared Sensor Arrays

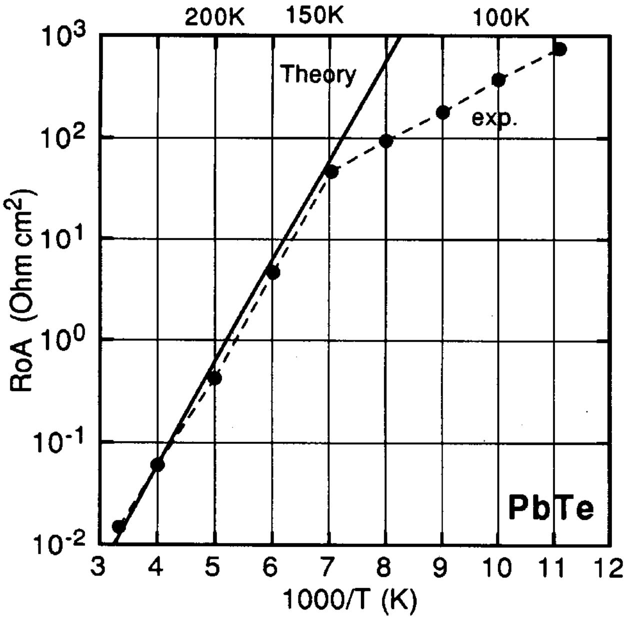
The lead-chalcogenide layers such as $Pb_{1-x}Sn_xSe$ and PbTe with band gaps of 0.1- 0.2 eV are grown by Molecular Beam Epitaxy (MBE). An intermediate CaF_2 buffer layer serves for compatibility. A two chamber MBE-system is used for this purpose. The quality of infrared devices critically depends on the quality of the layers. Contrary to narrow gap $Hg_{1-x}Cd_xTe$, dislocations in IV-VI layers can move easily along their main glide system at high and even at low temperatures. This behaviour can be used to improve the structural quality of the layers. Fig. 1 shows how dislocations moved towards the edges of a sample. The movement is caused by the thermal mismatch strain induced on temperature changes. Dislocation densities as low as 1 x 10^6 cm^{-2} and below were obtained after such anneals, and even on samples of several cm size. Keeping in mind that these values are obtained in 3 µm layers on heavily lattice mismatches substrates, these values compare favourably to HgCdTe layers on lattice matched CdZnTe substrates where dislocation densities of 10^5 cm^{-2} are observed. The Hall mobilities of PbTe and PbSnSe at low temperatures (<30K) are entirely determined by the density of dislocations. Values as high as 450'000 cm^2/Vsec have been obtained in these layers.
The layers are used to fabricate photovoltaic infrared sensor arrays for thermal imaging and spectroscopic applications. Fig. 2 shows the resistance-area product (essentially the inverse of the noise current density) as a function of temperature. The theoretical values as predicted by the Schottky-theory are obeyed down to about 100 K. Below this temperature, the change in slope is due to inhomogeneities of the Schottky barrier height.

Sponsor: Swiss NF, GRD, KTI

Fig. 1. Dislocation (etch pit) density in structured PbSe layers on Si(111) before (a) and after (b) a thermal anneal at 300°C.

Fig. 2. Resistance-Area product RoA of a PbTe Schottky barrier infrared photodiode (5.5 µm cut-off wavelength at 77K) as a function of temperature T. The maximum obtainable theoretical values are indicated as a solid line.





Heteroepitaxial high quality narrow gap lead-chalcogenides on Si(111) and formation of quantum dots

High quality epitaxial lead-chalcogenide layers like PbTe and PbSe are obtained on Si(111) substrates by molecular beam epitaxy. The large lattice mismatch as well as the thermal expansion mismatch lead to a high number of dislocation lines at and near the interface. Since dislocations are highly mobile in high quality lead-chalcogenides and due to the thermal mismatch, the threading ends of the misfit dislocations move on each temperature change in order to relieve the thermal mismatch strain. If two threading ends meet within a certain reaction distance, and if their Burgers vectors are appropriate, they react: They either annihilate, or fuse in a manner that only one dislocation is left. Therefore, the number of threading ends at the surface of the layer decreases on each temperature change. From the rate of the decrease, we calculated a reaction radius of about 7 nm.

For lead-chalcogenides, the low temperature saturation mobilities μ_{sat} are entirely determined by the dislocation densities (This is contrary to e.g. III-V semiconductors, where μ_{sat} is limited by impurity scattering).

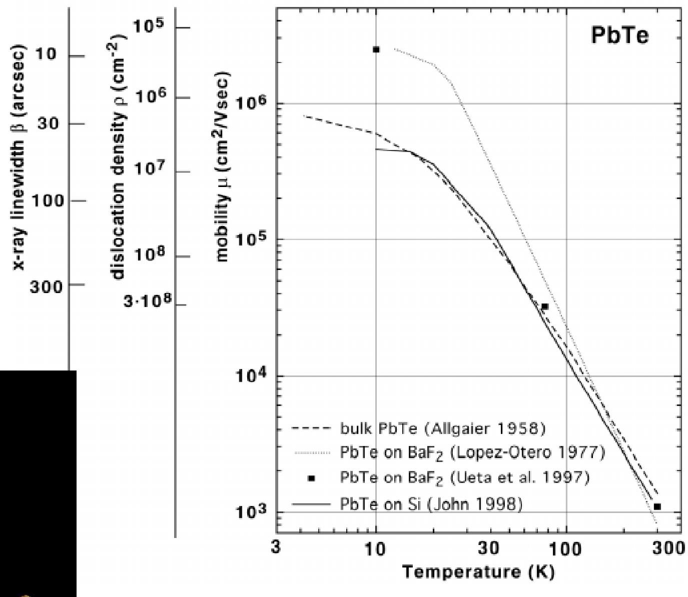
The highest μ_{sat} reported for lead-chalcogenides are as high as 3 x 10^6 cm^2/Vs and correspond to dislocation densities below 10^6 cm^{-2}. For our epitaxial layers on extremely lattice-mismatched Si(111) substrates , the highest μ_{sat} are still 200000 to 500000 cm^2/Vsec, this corresponds to dislocation densities in the mid 10^6 cm^{-2} range.

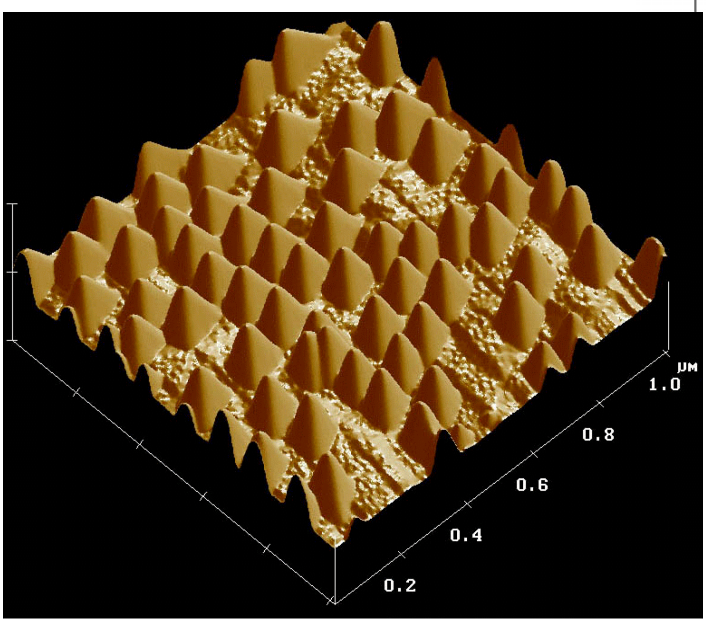
Layers with such dislocation densities allow the fabrication of infrared devices (see accompagnying contributions) as well as of well oriented quantum dots: If the PbTe layer is overgrown with a suitable amount of PbSe (lattice mismatch 5%), equally oriented dots with triangular side faces corresponding to (100) planes form with near uniform sizes. Such dots are of interest for optoelectronic applications like quantum dot emitters.

Figs.:
Right: Mobilities of PbTe as a function of temperature and correlation with dislocation densities and x-ray line widths.

Bottom: AFM image of PbSe on PbTe(100) quantum dots. The side faces of the dots correspond to (100) planes

Sponsor: Swiss NF



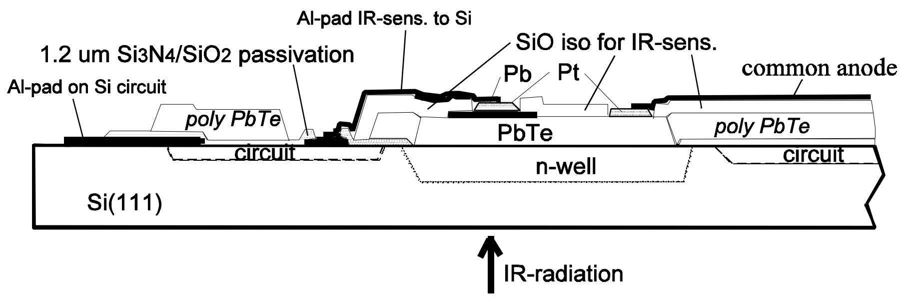


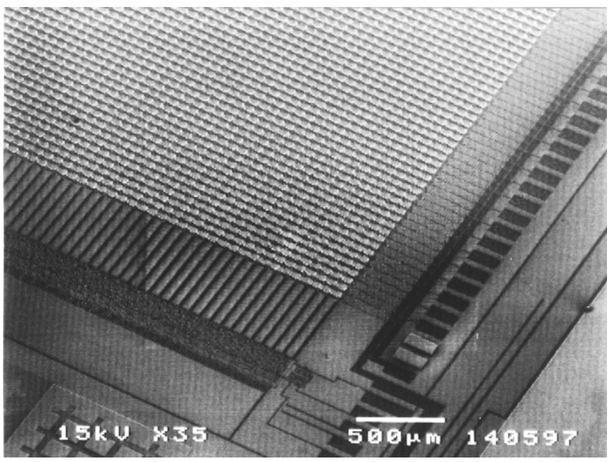
Monolithic Two-Dimensional PbTe Infrared Sensor Array on a Read-Out Si-Chip

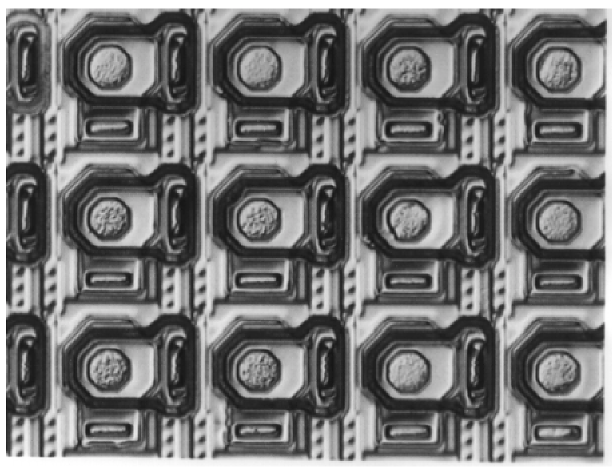
The highest sensitivities of infrared sensors for thermal imaging are obtained with narrow gap semiconductors. Infrared focal plane arrays employing such semiconductor sensor pixels are presently fabricated in a hybrid manner: The chip containing the 2-d arrays is fabricated in a suitable narrow gap material like HgCdTe or InSb, while the read-out multiplexer is constructed with Si technology. Hybrid connections are usually formed by indium bumps for each individual pixel. This makes the technique rather expensive for 2-d sensor arrays containing many thousands of pixels.
Due to the easy molecular beam epitaxy of narrow gap PbTe and $Pb_{1-x}Sn_xSe$ layers on Si(111)-substrates, a monolithic design becomes possible by growing the infrared sensor material as a thin layer directly onto the Si read-out chip. For practical reasons, postprocessing is used, i.e. the Si-chip is completely fabricated and tested before the sensor layer is deposited. Such devices have not been realized up to now.
For our demonstration, a special read-out chips with 128 x 96 pixels on a 75 µm pitch was fabricated in JFET/CMOS technology on backside polished Si(111). The chip contains a switching transistor for each individual pixel, and a shift register to access the lines serially. The columns are fed out in parallel to a separate amplifier chip. The design and fabrication was done by W. Buttler, Essen, and Fraunhofer-Institut Duisburg, respectively.
Layers of PbTe with about 3 µm thickness are grown by molecular beam epitaxy onto the read-out chip. The temperature budget does not exceed 450°C for 1 h because of the Al-metallization. The PbTe-layer is etched to individual pixels and sensors are fabricated. The blocking Pb-contacts as well as the ohmic contacts and Al-fan-out are delineated by lift-off techniques. As insulator layer, a photosensitive polyimide is employed, and RIE serves for openings in the Si3N4/SiO2 passivation layer of the read-out chip.
Presently, all these steps are developed, and a few arrays were successfully processed for the first time.

Sponsor: GRD

Figs. Schematic cross section, part of the 2-d array, and some individual pixels after complete processing





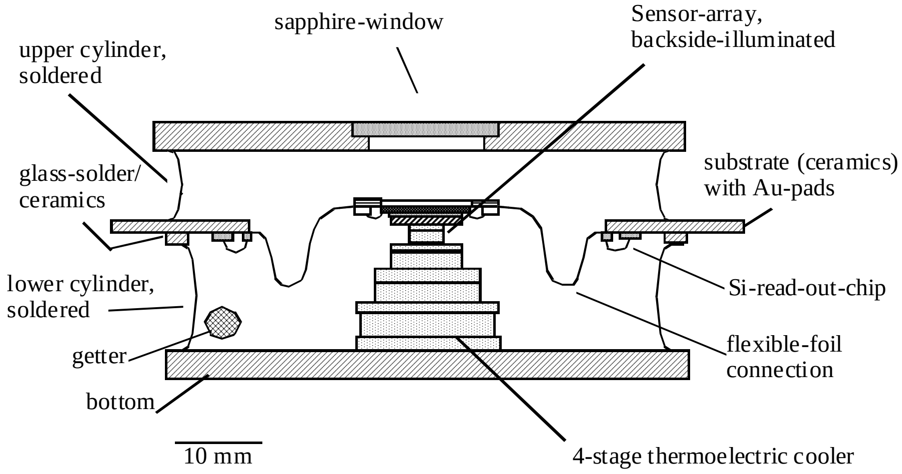


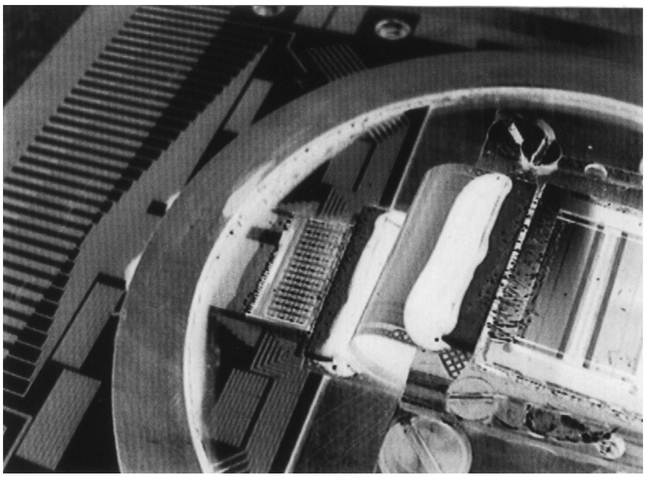
Packaging of Thermoelectrically Cooled Infrared Sensor Array

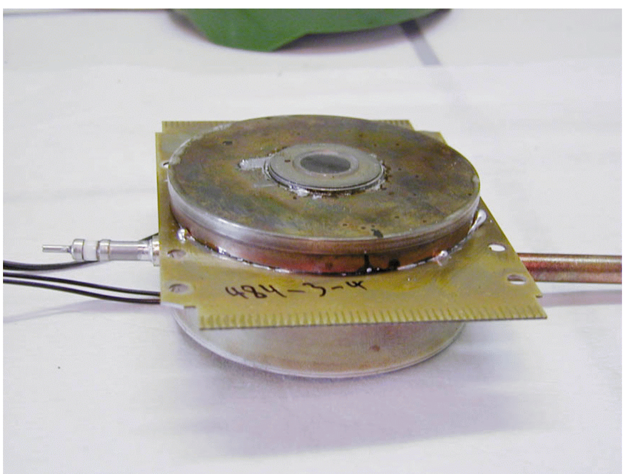
While sensitive semiconductor infrared sensor arrays for the atmospheric 8-12 µm window have to be cooled to below 130K, thermoelctric cooling can be employed for certain applications for sensors operating in the 3-5 µm wavelength range. A compact sealed package for a thermoelectrically cooled linear PbTe infrared sensor array sensitive in the 3-5 µm range was designed and realized. The sensor array contains 128 pixels and is soldered onto a 4-stage thermoelectric cooler. The two read-out chips each containing 64 parallel low-noise integrators and one serial analog output are bonded on a ceramic substrate and operated at room temperature.
The electrical connections between the cooled sensor pixels and the inputs of the amplifiers are realized with a novel low thermal conductivity flexible kapton foil which contains thin film gold leads as conductors.
The electrical connections to the outside world are formed on the same ceramic substrate with the aid of novel planar thin-film feed-throughs. The pitch of the Au-pads serving as feed throughs is 250 µm. For electrical insulation, a low temperature glass solder is used which solders the substrates containing the electric lines to a ceramic ring (see figures). The top of the package with a sapphire window as well as the bottom onto which the high temperature side of the thermoelectric cooler is soldered complete the package. The solderings have to be performed with different low temperature alloys since the thermoelectric coolers do not withstand temperatures higher than 138 °C.
A nonevaporable getter is used to maintain the vacuum. The sensor array and package are fully operative, a sensor temperature below -66°C is reached.
The soldering techniques were developed in collaboration with B. Zigerlig, GVE-EMPA group (formerly at AFIF).

Figures.: Cross section of the encapsulation, part of the ceramic substrate and the IR-array, completed package.

Sponsor: KTI







Infrared p-n junction sensors in epitaxial PbTe on Si(111) structures

The sensitivity of infrared sensors for thermal imaging applications is determined by their noise currents. The ultimate theoretical limit of narrow bandgap p-n junction infrared sensors is the diffusion limit, determined by band-to-band recombination (and can be attained in practice, contrary to larger bandgap devices where g-r recombination dominates). For Schottky barrier infrared sensors (as described on the preceding page), the ultimate limit is given by the standard Schottky theory. We already observe this limit over a large temperature range (300K to 150K) in our best sensor arrays (grown by molecular beam epitaxy on lattice mismatched Si(111) substrates). However, the theoretical diffusion limit for p-n junctions is still near 10 times better. We therefore fabricated p-n junctions in such PbTe layers. Fig. 1 shows a schematic cross section of an individual pixel. The noise currents we observed so far are not at the diffusion limit (solid line in fig. 2), but follow the g-r limit, however. The carrier lifetime is calculated from the experimental results and amounts to ~10 nsec. This corresponds to a diffusion length of ~0.7 µm.

The threading dislocation density in the layer used for the fabrication was around 10^8 cm^{-2}. This corresponds to a mean spacing between threading dislocations terminating at the surface of ~0.8 µm, just the same value as the diffusion length. We therefore can conclude that the threading dislocations are entirely responsible for the observed additional noise currents, and can extrapolate that a decrease to 10^6 cm^{-2} density is needed to obtain the theoretical diffusion limit down to ~180K. For the Schottky barrier devices of the same type, an about 10 times higher dislocation density is tolerable to still obtain the theoretical limit. Therefore, the lower noise current in p-n junctions has to be payed with a lower dislocation density. We already have obtained dislocation densities of 10^6 cm^{-2} in lead-chalcogenide on Si(111) layers, but have not yet fabricated devices in these layers, however.

Sponsor: KTI, GRD

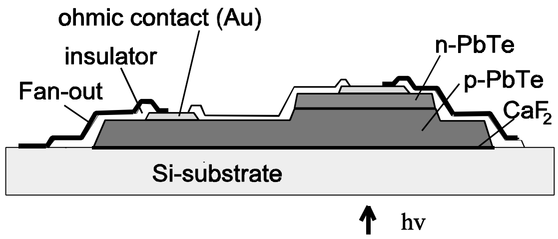
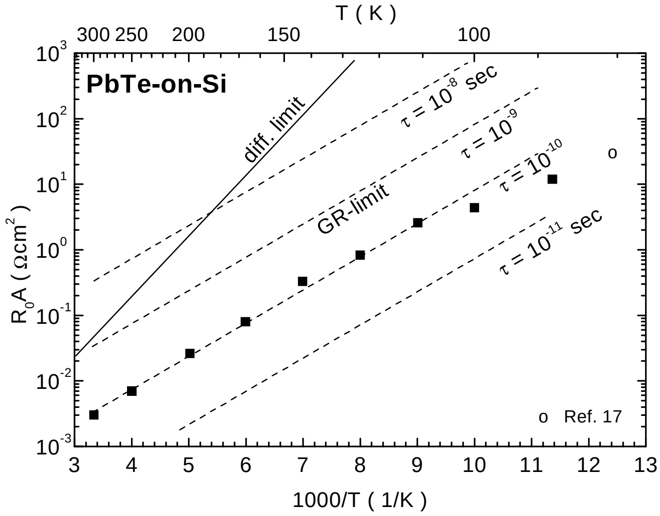


Fig. 1 . Cross section of a p-n IR photodiode fabricated in an epitaxial PbTe-on-Si layer

Fig. 2. Differential resistance area products RoA (~inverse noise currents) for a p-n PbTe-on-Si IR photodiode. Theoretical diffusion limit (diff.) and experimental results with corresponding g-r lifetimes.



Lightweight and flexible $Cu(In,Ga)Se_2$ solar cells on polymer with a world record efficiency of 12.8%

Development of high efficiency, stable, lightweight and flexible solar cells is important for novel applications. The $Cu(In,Ga)Se_2$ (called CIGS) solar cells have a potential to yield solar electricity at a low cost of < 1 Euro/Wp. The CIGS solar cells are also promising for space applications because their stability against high energy irradiation are superior to crystalline Si and GaAs solar cells. The CIGS solar cells on polymers can yield a very high specific power (defined as ratio of out-put power to weight of solar module) of about 1.5 kW/Kg, which is 3-4 times higher than in conventional Si cells.

Typical CIGS absorber layers for high efficiency solar cells are grown on Mo coated soda-lime glass substrates at a temperature of about 550 °C. A certain amount of Na and high deposition temperatures are required for an optimum carrier concentration and large grain size of the CIGS absorber layers. None of the polymers known up to now can withstand such a high temperature. Most of the commercially available polymer sheets are recommended to be used below 350 °C. Moreover, these polymers do not contain Na. Because of the lower substrate temperature and non-availability of Na during the growth of CIGS absorber layers low efficiency solar cells are therefore expected on polymers.

A lift-off process has been developed to obtain CIGS solar cells on lightweight and flexible polymer films (see fig. 1). The absorber layer is grown by a co-evaporation method on a polyimide layer, which is spin coated on a NaCl covered glass substrate. The NaCl intermediate layer can provide Na to the $Cu(In,Ga)Se_2$ layer during deposition. After the complete processing of the cells, the NaCl buffer layer is dissolved to separate the glass substrate from the $ZnO/CdS/Cu(In,Ga)Se_2/Mo$/Polyimide stack. The total thickness of the solar cell including polymer substrate is less than 25 microns. A record conversion efficiency of 12.8% (total area, no antireflection coating) was independently measured at FhG/ISE, Freiburg, Germany. This is the highest reported efficiency for any type of solar cell grown on polymers.

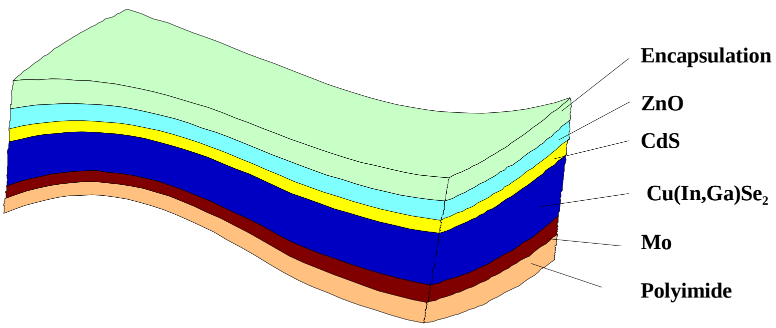


Figure 1: Schematic diagram of the ZnO/CdS/CIGS/Mo/polyimide flexible solar cell.

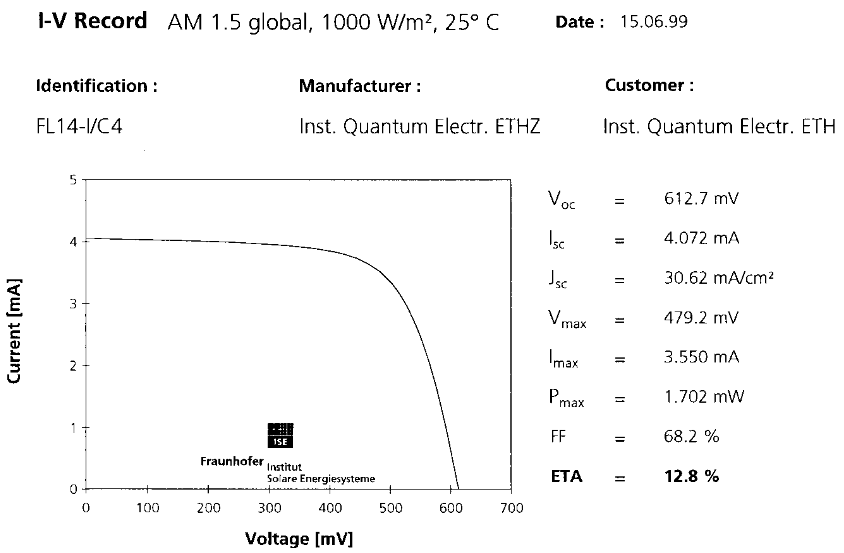


Figure 2: I-V characteristic of a 12.8% efficiency CIGS solar cell on polyimide layer measured under AM1.5 illumination at FhG/ISE, Freiburg, Germany.

Growth and characterization of heteroepitaxial $CuIn_ySe_y$ layers and interfaces

Chalcopyrite ($CuInSe_2$) and defect-chalcopyrite (different In-rich $CuIn_xSe_y$ compositions) compounds are important materials for stable and high efficiency polycrystalline thin film solar cells. Heteroepitaxial layers of $CuIn_xSe_y$ are grown on Si and GaAs substrates by molecular beam epitaxy. Despite of large lattice mismatch and different thermal expansion coefficients, epitaxial layers of "good structural quality" have been obtained. X-ray diffraction (XRD) measurements and the analyses of the lattice vibrational properties by Raman scattering and infrared absorption show (fig. 1) that the $CuIn_{2.5}Se_4$ (β-phase), $CuIn_3Se_5$, and $CuInSe_2$ are single phase compounds while $CuIn_{1.6}Se_{2.9}$ is a mixture of $CuInSe_2$ (α-phase)and $CuIn_{2.5}Se_4$ (β-phase) compound

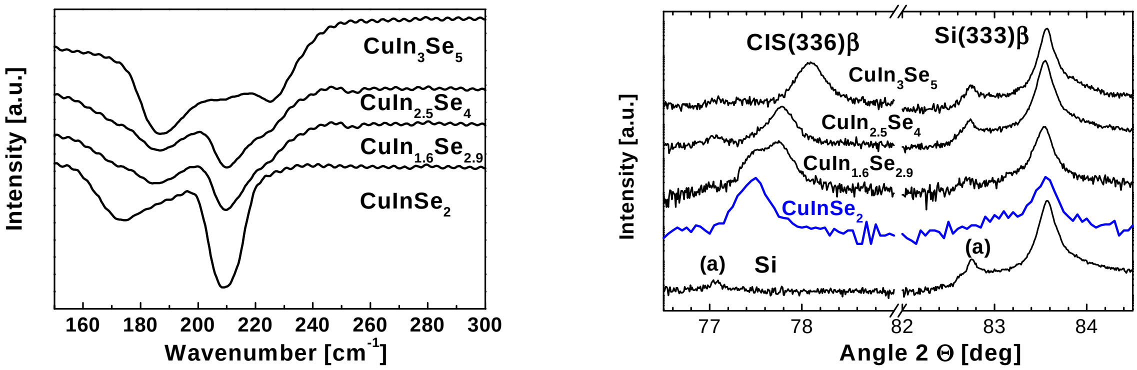


Figure 1: IR-absorption spectra and XRD of epitaxial $CuIn_xSe_y$/Si(111) layers.

Transmission electron microscopy (TEM), Rutherford backscattering spectroscopy and XRD were used to investigate the substrate-layer interfaces. In the case of $CuIn_xSe_y$/Si an interfacial $CuSi_xSe_y$ layer is formed during the growth of epitaxial layer. However, for $CuIn_xSe_y$/GaAs, a strong diffusion of Ga into the $CuIn_xSe_y$ is observed. Formation of the $Cu(In,Ga)Se_2$ compound and microstructural defects at the $CuInSe_2$-GaAs interface have been identified (see fig. 2).

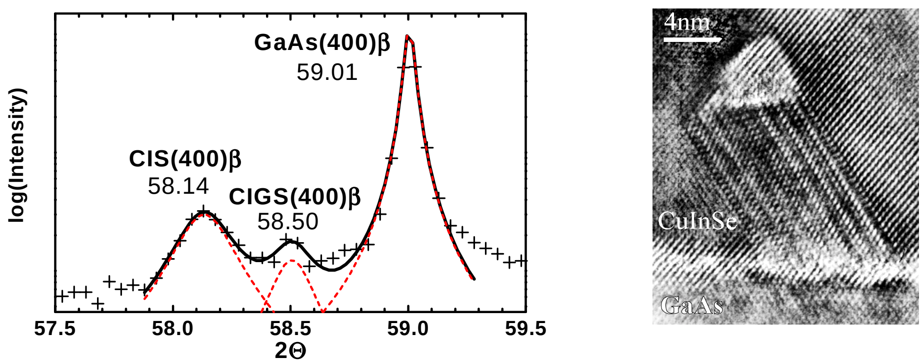


Figure 2: XRD and high resolution cross-sectional TEM of $CuIn_xSe_y$/GaAs show the formation of an interfacial $Cu(In,Ga)Se_2$ compound and microstructural defect.

Chemical bath deposition (CBD) process for the growth of n- type wide band gap (2.4 eV) CdS layers has been installed. In collaboration with the group of Dr. Lincot, ENSCP, Paris, epitaxial growth of CdS on single crystal $CuInSe_2$/Si was achieved for the first time by CBD. TEM measurements show the importance of the etching of $CuInSe_2$ surface to obtain CdS layers with less structural defects.

Sponsors: NF, PSEL, BBW/EU

Chalcopyrites for advanced thin film solar cells

The objective of the project is to develop tandem or composition graded polycrystalline thin film solar cells based on $CuGa_xSe_y$ (Eg=1.68 eV) and $Cu(In,Ga)Se_2$ (Eg=1.0-1.2 eV) layers grown by a physical vapor deposition process.

This required the development of a chemical bath deposition process for the growth of n-type CdS window layers and the deposition of ZnO as a transparent conducting electrode.

A rf magnetron sputtering system has been installed and the growth conditions have been optimized to grow highly transparent (about 85% transparency in the VIS-NIR spectrum) and conducting (about 10 Ω/□) ZnO:Al and ZnO layers.

Solar cells in the superstrate and substrate configuration have been grown on ZnO:Al/ glass and Mo/glass substrates, respectively. The work on $CuGa_xSe_y$/ZnO superstrate solar cells is in the initial stage. However, we have developed a process for the growth of $Cu(In,Ga)Se_2$ layers on Mo/glass with "optimum" composition profile and a "good" microstructure. ZnO/CdS/$Cu(In,Ga)Se_2$/Mo/glass solar cells with conversion efficiencies in the range of 14 to 16% have been fabricated. Figure 1 shows a SEM cross-section image and I-V characteristic of a $Cu(In,Ga)Se_2$ solar cell in the substrate configuration.

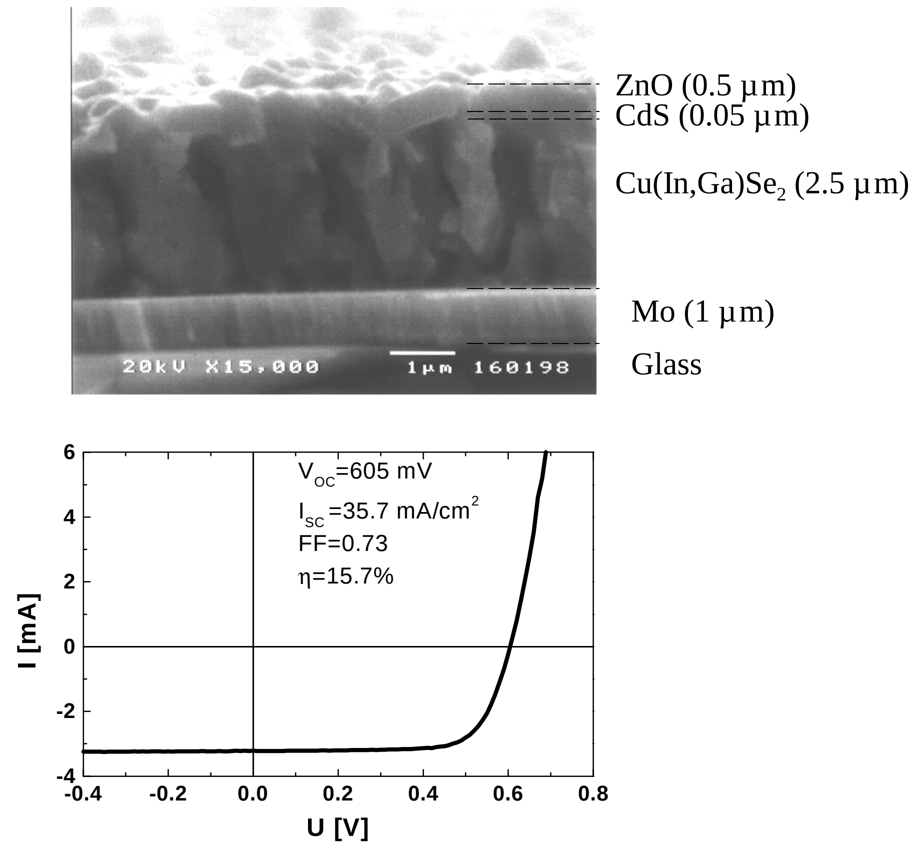


Figure 1: SEM cross-section and I-V characteristics of a 15.7% efficiency thin film polycrystalline $Cu(In,Ga)Se_2$ solar cell.

Sponsor: BBW/EU (JOULE project)

CdTe/CdS thin film solar cells

CdTe/CdS photovoltaic modules are in the advance stage of development for industrial production of high efficiency, stable, environmentally safe and economical source of solar electricity. In collaboration with industries such as BP Solar Ltd, PHILIPS, ANTEC GmbH, and SOLARONIX we are working on the following topics:

1. Increase the growth rate and large uniformity of CdTe and CdS layers for fast processing of solar cells for industrial production.
2. Novel materials and processes for improving the performance of "ohmic back contact" to CdTe for high efficiency and long term stability.
3. Understanding the opto-electronic properties and recrystallization phenomena in CdTe and CdS thin films. Structural and electrical transport properties of heterojunctions.

CdTe/ CdS solar cells are grown on transparent conducting oxide (TCO) coated glass substrates by a process in which all the layers (CdTe, CdS, $CdCl_2$, and ohmic back contact) are grown by vacuum evaporation methods. Different type of TCO's (ITO, FTO and ZnO) are evaluated for their application as a transparent electrode. Solar cell efficiency depends on the "$CdCl_2$ treatment" used for the recrystallization of CdTe. As-deposited CdTe layers have small grains in the range of 0.5 to 1 µm. However, after the $CdCl_2$ treatment a large increase in the grain size of CdTe is observed (see figure 1) and a loss of the (111) preferred orientation (reduced texturing) is measured with x-ray diffraction. The solar cell properties depend on the recrystallization of CdTe layers and TCO substrate (see figure 2).

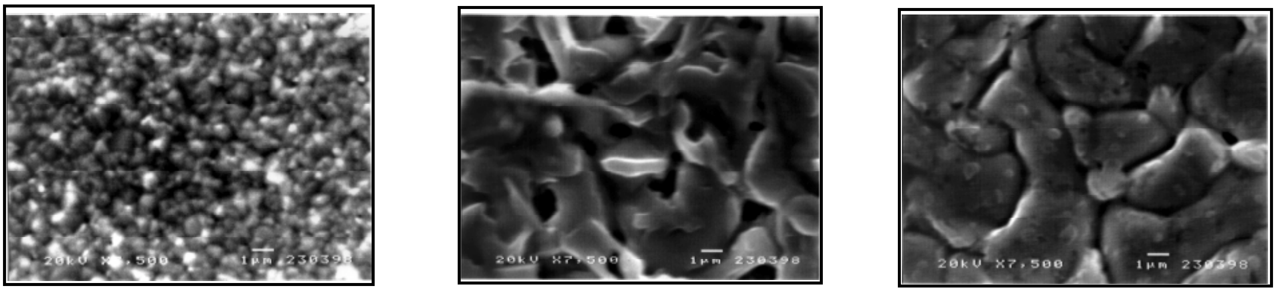


Figure 1: Morphology of as-deposited and recrystallized CdTe layers on ITO (left and middle) and recrystallized CdTe on FTO (right) substrates.

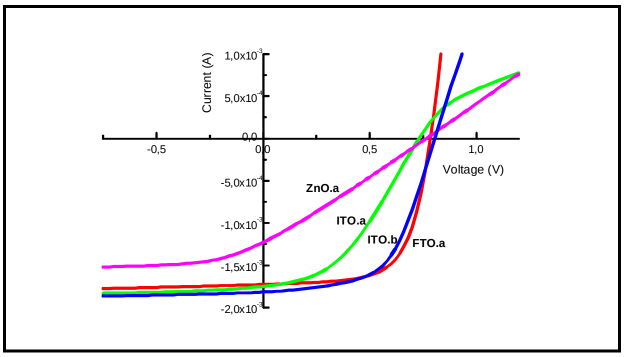


Figure 2: I-V curve of CdTe/CdS solar cells on different TCOs. CdTe is recrystallized with a: 600 nm $CdCl_2$ and b: 60 nm $CdCl_2$. Solar cell efficiency on ITO is 10.4% and 11.5% on FTO.

Sponsor: BBW/EU (JOULE Project)

Broadband semiconductor Bragg mirror and saturable absorber for ultrashort laser pulse generation

Conventional semiconductor saturable absorber mirrors (SESAM) for solid state lasers limit further pulse shortening due to the relatively small reflection bandwidth of the semiconductor Bragg mirrors. To overcome the refractive index limitation, III-V/IIa fluoride material pairs have been introduced, which have refractive index ratios up to a value of 2.3.

Bragg mirrors and saturable absorbers consisting of four (Ga,Al)As/CaF_2 stacks have been grown for various center wavelengths by molecular beam epitaxy (MBE). Mirror-like surfaces were obtained. Problems with layer cracking due to high thermal strain in the fluoride layers during cooling down have been solved by applying temperature cycling during growth. Such Bragg mirrors, designed for a center wavelength of 750 nm, provided more than twice as much spectral bandwidth compared to that of the original semiconductor Bragg mirrors con-sisting of (Ga,Al)As/AlAs. The maximum reflectivity of 98.5% is comparable to that of silver mirrors. SESAM's have been grown by adding spacer and absorber layers on top of such a Bragg mirror structure. The reflectance spectrum of an absorber mirror, with a center wavelength of 780 nm and a reflectivity higher 98%, is shown in Fig. 1. SESAM's are evaluated in terms of their modelocking efficiency in cw-pumped Ti:sapphire lasers. The goal is to produce ultrashort sub-10 fs pulses and broadly tunable femtosecond pulses.

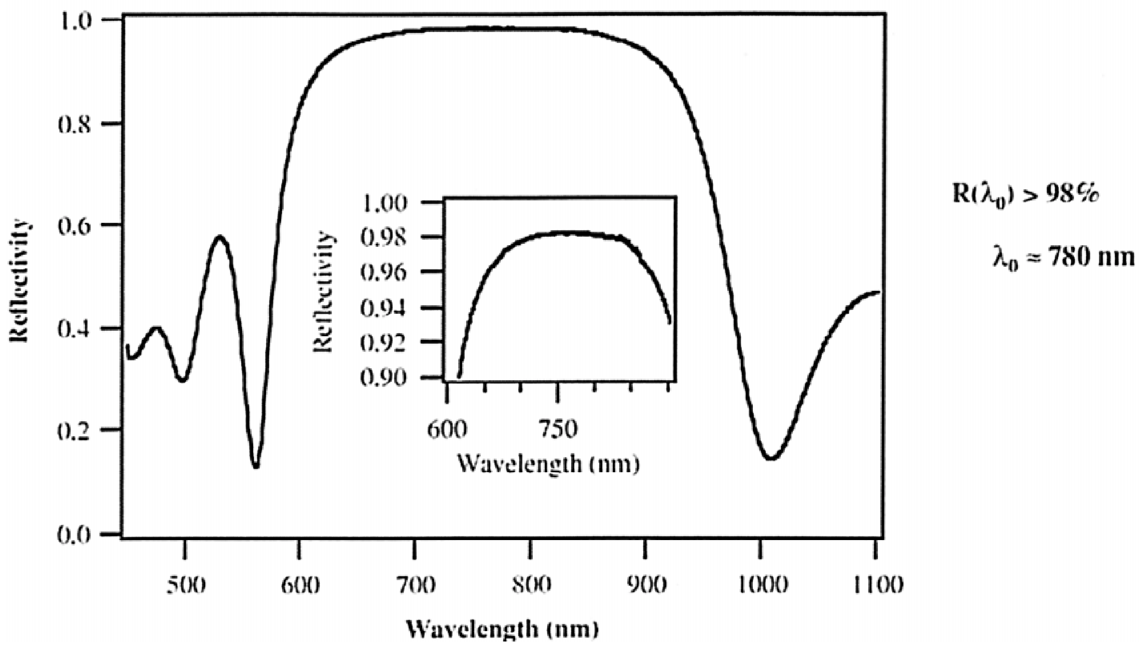


Fig. 1. Reflectance spectrum of a broadband saturable absorber mirror (SESAM) centered at 780 nm wavelength and consisting of 4 epitaxial CaF_2/GaAlAs quarter wavelength stacks. Complete spectrum and high reflectance part (inset).

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H. Zogg, K. Alchalabi, A.N. Tiwari
Photovoltaic IV-VI on silicon infrared devices for thermal imaging applications
IWPSD, Tenth International Workshop on Physics of Semiconductor Devices,
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